Amendments to the Drawings:

Please amend the Figures 2A, 2B, 2C, 2D, 2E, 3A, 3B, 3C, 4A, 4B, 4C, 4D, 4E, 4F, 4G, 4H, 4I, 4J, 5C, 5D, 5E, 5F, 6, 7A, 7B and 8 as shown in red ink on the prints accompanying this amendment.

The drawings have been amended to add or delete numerals and lead lines in the areas noted by the Examiner in paragraphs 1 and 2 of the Office Action.

Attachments: Proposed Drawings as listed above.

REMARKS/ARGUMENTS

The specification and drawings have been amended to correct the errors noted by the Examiner. The Abstract has been shortened. Claims 9 and 18 have been amended to clarify them.

Claims 1 - 82 are pending in the application.

Traversal of the Prior Art Rejection

The rejection of claims 1, 3 - 8, 11, 13, 15 and 16 under 35 U.S.C. §102(b) as being anticipated by Ahanin et al (US 5,166,604) (hereinafter "Ahanin") is respectfully traversed. In the effort to read Ahanin's disclosure on applicants' claims, the Examiner relies on Ahanin Figure 1 ("prior art"). The Examiner refers to column 2, lines 22 - 52 of Ahanin. However, Ahanin then states that: "The foregoing test method can generally not be used for asynchronous logic circuitry..." (col. lines 53-54). Thus, the Examiner's 35 U.S.C. §102 anticipation rejection based on column 2, lines 22-52 and Figure 1 of Ahanin for background and for the capture operation is flawed on its face.

More importantly, in applicants' Figs. 2B - 2E and in the text of the specification at pages 5 - 8, four prior art solutions are set out in detail with their advantages and disadvantages. Applicants respectfully submit that Ahanin is in the category of applicants' prior art solution #4 (see FIG. 2E) and has the same defect thereof as set out in applicants' specification at the paragraph bridging pages 7 and 8. Prior art #4 uses only one

additional input, called ESR_EN, for each asynchronous set/reset port, which is the same as that used on US 5,166,604. The present invention, however, used two pins, called global_SE and global_SR_EN, for each asynchronous set/reset port to switch from shift mode to capture mode and *vice versa*, see FIG. 3A. Thus, applicants respectfully submit that Ahanin does not show or suggest the shifting-in, capturing and shifting-out as set out in applicants' claim 1; especially clause (b):

> capturing a test response of all said scan cells for testing said faults propagated to said data ports and said asynchronous set/reset ports of all said selected scan cells by enabling or disabling all said set/reset enable (SR_EN) signals connected to all said selected scan cells during a capture operation...."

Claims 2-16 depend from claim 1 and are patentable for the same reason.

The rejection of claims 10 and 17 - 30 under 35 U.S.C. §103(a) as being unpatentable over Ahanin in view of applicants' own prior art of FIG. 2D is respectfully traversed.

As shown above, Ahanin is using the same approach as described in applicants' application and characterized as prior art #4 and shown in Figure 2E. Thus Ahanin uses only one additional input called the ESR_EN, for each asynchronous set/reset port. The present invention, however, uses two pins called global_SE and global_ SR_EN, for each asynchronous set/reset port to switch from shift mode to capture mode and vice versa as shown in FIG. 3A.

Hence, applicants respectfully submit that claims 10 and 17-30 are patentable over the art for the reasons given above.

The rejection of claims 31-82 under 35 U.S.C. §103(a) as being unpatentable over Ahanin (US 5,166,604) in view of applicants' own prior art FIG. 2D further in view of Ruiz et al (US 6,195,776) is respectfully traversed. As shown above, Ahanin is in the category of applicants' prior art #4 using one additional input called ESR_EN, for each asynchronous set/reset port. In applicants' application, two pins, called global_SE and global_SR_EN, are used for each asynchronous set/reset port to switch from shift mode to capture mode and *vice versa* as shown in FIG. 3A of applicants' drawings and described in applicants' specification. Applicants' prior art #3, FIG. 2D, uses scans in a scan enable signal to disable the asynchronous set/reset ports of all the scans held during the shift operation for the complete duration of the scan test or self-test. As stated at page 6 of applicants' specification:

" This solution repairs the asynchronous set/reset violations by adding an AND gate and an inverter to force all asynchronous set/reset ports into an inactive state using the scan enable (SE) signal in scan-test or self-test mode, while allowing the functional set/reset signals to drive the asynchronous set/reset ports during the capture operation as well as during normal operation. This guarantees that the asynchronous set/reset ports of all scan cells are disabled during the shift operation allowing the scan chains to operate correctly as a shift register. The advantage of this solution is that the faults present in the functional circuitry driving the asynchronous set/reset ports of all scan cells can now be propagated and tested during the capture operation resulting in no fault coverage loss as compared to prior-art solutions #1 and #2. In practice however, problems occur when using this solution due to the race condition between the data and set/reset ports that occurs during the capture cycle. This can often result in an unreliable state being captured into the scan cells, followed by pattern mismatches during comparison or compaction, thus invalidating the test. "

From the above, it is clear that the third prior art solution of FIG. 2D does not supply the feature that the Examiner suggests it does. For these reasons, claims 31-82 are patentable over the art.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Applicants

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

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